Requisition #	BA204
Job Title	Design Engineer
Posting Date	2/15/2013
Job Area	Engineering - Hardware
Location	California – Silicon Valley
How to Respond	Email a cover letter and resume to **jobs@adapt-ip.com**
Company	**Adapt IP** is the most exciting semiconductor design company in the business – founded by seasoned professionals, at Adapt IP we use the newest methods develop cutting edge components for today's chipsets. Our techniques enable us to deliver reduced development time, targeted performance, and the best bill-of-material cost in the industry.
Responsibilities	You will be a part of the design implementation team responsible for developing SystemC synthesizable designs for cutting edge technologies. You will work with the customer to capture and develop design specifications and drive the micro-architecture of portions of the model design. You will refine and synthesize these models into FPGA and ASIC implementations for our systems companies, employing high level synthesis tools to meet the design specifications for area, timing and power requirements. You will implement and deliver RTL and will work with verification engineers to develop unit-level and integrated-level test benches. Using these platforms, you will be responsible for debugging your designs in stand-alone mode and also when integrated with the rest of the core IP and ultimately with the rest of the chip. You may also be responsible for synthesis and gate-level timing tasks related to your module and will assist with verification and timing closure. You will make regular contributions to the overall improvement in design methodology to drive productivity and quality of result.
Desired Skills and Experience	• Experience using high level synthesis tools required. • SystemC experience both in model creation and in high level synthesis • Experience with Verilog and/or VHDL ASIC design • Familiarity with leading edge RTL and gate level verification techniques. • Knowledge of digital signal processing techniques is a plus. • Experience with FPGA tools chains is useful. • Knowledge in implementing multi-domain clock synchronization, pipelining, and low-power design techniques. • Must have worked on at least one design with direct participation in micro-architecture and logic design through tape out. • Innovative, self-directed and self-motivated team player able to thrive in a fast-paced, organic engineering environment. • Experience with developing, tracking, and achieving project schedules. • Good verbal and written communication skills.
Education Requirements	Required: Bachelor's, Electrical Engineering or equivalent experience Preferred: Master's, Electrical Engineering or equivalent experience
Keywords	SystemC, High Level Synthesis, Verilog, VHDL, ASIC, FPGA