Adapt IP

We make standard IP *fit your needs*

USB 3.0 Super Speed Device Core

AIP-USB3.0-4D-AXI

OVERVIEW

The **Adapt-IP Super Speed Device Core** IP provides the designer with Super Speed device performance in a customizable, small footprint suitable for both FPGA and ASIC designs. Packaged as a component for both the Altera Qsys and Xilinx EDK flows, the core can be added to a FPGA design in minutes. For SoC flows, we tune the Adapt-IP core for **your technology library**.

Complete supporting **firmware** including mass storage device class support for both Linux and Micrium is provided in source code form. Other RTOS will be supported on request. The core and firmware will be Logo Certified as a USB 3.0 Super Speed device by the USB Implementer's Forum.

Customization is a key feature of the core's design. Adapt-IP can configure the number of concurrently active endpoints, the microprocessor bus interface, and the size of the FIFO buffer memory to meet customer needs. Adapt-IP can add unique and/or advanced features such as in-line real time compression / decompression and encryption to any or all endpoints.

The Adapt-IP Super Speed Device Core in standard configuration **supports 4 simultaneous input and 4 output endpoints**. Bulk burst transactions run at maximum Super Speed rates and use DMA to and from the microprocessor bus to achieve this throughput. Adapt IP can configure the core with additional, or fewer endpoints to meet your design goals.

In standard configuration **AXI is the bus interface** connecting the Adapt-IP Super Speed Device core to the device's compute system as both a slave for configuration purposes and as a master with DMA for endpoint data transfer. Other appropriate buses can be supported at customer request.

The Adapt-IP Super Speed Device core will work with any **PIPE 3 compatible PHY**.

The Adapt-IP Super Speed Device core will work with any USB2 or USB 1 device controller, including the **Adapt-IP USB2.0 High Speed Device Core**.

A Programmer's View **Virtual Platform** model of the AIP-USB3.0-4D-AXI is available enabling easy device bring up on a Virtual Platform.

Deliverables

- Altera Qsys component
- Xilinx EDK component *or*
- SoC Synthesizable Verilog
- Linux firmware *or*
- Micrium firmware
- Logo Certification
- Virtual Platform model

Standard Features

- 4 input endpoints
- 4 output endpoints
- AXI Bus interface
- PIPE 3 PHY support
- Device Driver
- Virtual Platform model

Optional Features

- Additional/fewer inputs
- Additional/fewer outputs
- Alternate Bus interface
- Alternate PHY support
- Alternate Device Drivers
- Data compression
- Forward Error Correction
- *Plus Your Requested Feature*

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