Adapt IP

We make standard IP *fit your needs*

USB 2.0 High Speed Device Core

AIP-USB2.0-7D-AXI

OVERVIEW

The **Adapt-IP High Speed Device Core** IP provides the designer with High Speed and Full Speed device performance in a customizable, small footprint suitable for both FPGA and ASIC designs. Packaged as a component for both the **Altera** Qsys and **Xilinx** EDK flows, the core can be added to a FPGA design in minutes. For **SoC** flows, we tune the Adapt-IP core for **your technology library**.

Complete supporting **firmware** for standalone and FPGA vendor RTOS as well as for Windows XP/Vista is provided in source code form. Drivers for Linux and Windows are provided for SoC implementations. The core and firmware is Logo Certified as a USB 2.0 High Speed device by the USB Implementer's Forum, using the SMSC 3300 USB ULPI PHY.

Customization is a key feature of the core's design. Adapt-IP can configure the number of concurrently active endpoints, the microprocessor bus interface, and the size of the FIFO buffer memory to meet customer needs. The number of active endpoints can adjusted at runtime. Each endpoint supports bulk and interrupt protocol, and can be IN or OUT. The core's programmable ping-pong buffers are per each endpoint, and use on-chip dual port RAM. General isochronous support is provided for Full-Speed, and is an option for High Speed. Bus and core clocks are completely asynchronous.

Download Dual Port RAM Template

Supports **Xilinx Virtex 1 - Virtex 6 and Spartan 3 - Spartan 6.** Size is 750 slices on most devices. Supports Microblaze LMB and AXI buses. Peak performance is 52 MB/sec sustained with Microblaze running at 100MHz. Standalone & Xilinx Kernal RTOS firmware provided.
Download the Xilinx Core Template. **Download Xilinx User Manual.**

Supports **Altera Cyclone, Cyclone II and III and Stratix, Stratix II and Stratix GX.** Size is 1500 LE's on most devices. Supports Avalon bus. Uses Tri-Matrix as buffer memory. 19 MB/sec sustained transfer rates over USB. Standalone and UCOS 2 RTOS firmware provided.
Download the Altera Core Template. **Download Altera User manual**.

The Adapt-IP High Speed Device core will work with any **ULPI compatible PHY** and has been certified with the SMSC 3300 USB ULPI PHY.

The Adapt-IP High Speed Device core will work with any USB3 device controller, including the **Adapt-IP USB3.0 High Speed Device Core**.

Deliverables

- Altera SOPC component
- Xilinx EDK component *or*
- SoC Synthesizable Verilog
- Linux firmware
- Windows XP/Vista *or*
- FPGA firmware
- Logo Certification
- Virtual Platform model

Standard Features

- 7 user endpoints
- Designer configurable RAM
- ULPI PHY support
- Device Driver
- Virtual Platform model

Optional Features

- Additional/fewer inputs
- Additional/fewer outputs
- Alternate Bus interface
- Alternate PHY support
- Alternate Device Drivers
- Data compression
- Forward Error Correction
- *Plus Your Requested Feature*

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